WHAT IS CLAIMED IS:

1. A method for recovering a basic input/output system (BIOS) memory circuit in a computer system, comprising steps of:

providing a memory device comprising a first basic input/output system memory circuit and a second basic input/output system memory circuit, said first basic input/output system memory circuit and said second basic input/output system memory circuit respectively having a first computer program and a second computer program stored therein, wherein said first basic input/output system memory circuit and said second basic input/output system memory circuit are employed to initiate an operation of said computer system;

enabling said second basic input/output system memory circuit upon booting said computer system;

detecting if said first computer program includes an error; and

re-programming said first basic input/output system memory circuit based on said second computer program when said error is detected in said first computer program.

2. A method according to claim 1 wherein said first computer program and said second computer program are identical.

3. A method according to claim 1 wherein said first computer program and said second computer program are different.

4. A method according to claim 1 wherein said enabling step further comprises steps of:

providing a chip enabling circuit having a chip enabling control terminal; and

enabling said second BIOS memory circuit through said chip enabling

control terminal of said chip enabling circuit upon booting said computer system.

5. A method according to claim 4 wherein said chip enabling control terminal is a general purpose input/output pin (GPIO pin).

6. A method according to claim 1 wherein said detecting step further comprises steps of:

providing an error-detecting circuit; and

checking an error-detecting data value contained in said first computer program through said error-detecting circuit for determining if said first computer program includes said error.

7. A method according to claim 6 wherein said error-detecting data value is a checksum data value.

8. A method according to claim 6 wherein said error-detecting data value is a parity check data value.

9. A method according to claim 6 wherein said error-detecting data value is a cyclic redundancy check (CRC) data value.

10. A method according to claim 1 wherein said first basic input/output system memory circuit further comprises a flash utility for reprogramming said first basic input/output system memory circuit based on said second computer program.

11. A method according to claim 1 wherein said second basic input/output system memory circuit further comprises a flash utility for reprogramming said first basic input/output system memory circuit based on said second computer program.

12. A method for initiating a computer system, comprising steps of:

providing a memory chip comprising a first basic input/output system memory circuit and a second basic input/output system memory circuit, said first basic input/output system memory circuit and said second basic input/output system memory circuit respectively having a first computer program and a second computer program stored therein, wherein said first basic input/output system memory circuit and said second basic input/output system memory circuit are employed to initiate an operation of said computer system;

enabling said second basic input/output system memory circuit upon booting said computer system;

detecting if said first computer program includes an error;

re-programming said first basic input/output system memory circuit based on said second computer program when said error is detected in said first computer program;

enabling said first basic input/output system memory circuit and disabling said second basic input/output system memory circuit; and

initiating an operation of said computer system through said first basic input/output system memory circuit.

13. A method according to claim 12 wherein said first computer program and said second computer program are identical.

14. A method according to claim 12 wherein said first computer program and said second computer program are different.

15. A method according to claim 12 wherein said step of enabling said second BIOS memory circuit further comprises steps of:

providing a chip enabling circuit having a chip enabling control terminal; and

enabling said second BIOS memory circuit through said chip enabling control terminal of said chip enabling circuit upon booting said computer system.

16. A method according to claim 15 wherein said chip enabling control terminal is a general purpose input/output pin (GPIO pin).

17. A method according to claim 12 wherein said detecting step further comprises steps of:

providing an error-detecting circuit; and

checking an error-detecting data value contained in said first computer program through said error-detecting circuit for determining if said first computer program includes said error.

18. A method according to claim 17 wherein said error-detecting data value is a checksum data value.

19. A method according to claim 17 wherein said error-detecting data value is a parity check data value.

20. A method according to claim 17 wherein said error-detecting data value is a cyclic redundancy check (CRC) data value.

21. A method according to claim 12 wherein said first basic input/output system memory circuit further comprises a flash utility for reprogramming said first basic input/output system memory circuit based on said second computer program.

22. A method according to claim 12 wherein said second basic input/output system memory circuit further comprises a flash utility for reprogramming said first basic input/output system memory circuit based on said second computer program.